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10/708,638	03/17/2004	**Chi-Yang Lin**	V1AP0101USA	2637

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EXAMINER	
PIZIALI, JEFFREY J	
ART UNIT	**PAPER NUMBER**
2629	

NOTIFICATION DATE	DELIVERY MODE
07/09/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/708,638	LIN ET AL.	
	Examiner	Art Unit	
	JEFF PIZIALI	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10 and 19* is/are pending in the application.

4a) Of the above claim(s) *6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7-10 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings have not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the figures.

Specification

3. The amendment filed *26 March 2009* is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

"*As shown in Fig. 5, after the state machine 78 enters the operational state 96, the state machine stays in the operational state 96 for holding the setting value SET*" (see replacement paragraph 32).

The original disclosure does not lend support for the newly added subject matter of the state machine staying in the operational state 96 for holding the setting value SET after the state machine 78 enters the operational state 96.

Applicant is required to cancel the new matter in the reply to this Office Action.

4. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. *Claims 3-5, and 7-10* are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 3 recites, "***a state machine for generating a setting value according to the comparison result and outputting the setting value to the mirror ratio controller to adjust the mirror ratio***" (line 6).

Claim 9 recites, "***the state machine enters a first operating state for adjusting the setting value to drive the mirror ratio controller to lower the mirror ratio if the comparison result***

corresponds to a first logic level, and the state machine enters a second operating state for adjusting the setting value to drive the mirror ratio controller to raise the mirror ratio if the comparison result corresponds to a second logic level."

Claim 10 recites, "***the state machine will leave the first operating state and enter a third operating state for holding the setting value if the state machine is presently at the first operating state, and the comparison result corresponds to the second logic level, and the state machine will leave the second operating state and enter the third operating state for holding the setting value if the state machine is presently at the second operating state, and the comparison result corresponds to the first logic level.***"

However, the closest the originally presented specification ever comes to an enabling disclosure for making a "***state machine***" is this: "***Generally speaking, the state machine 78 is built by a plurality of flip-flops. After the state machine 96 enters the operational state 96, the state machine, therefore, stops flip-flops from being triggered to achieve the objective of holding the setting value SET***" (see Paragraph 32, Line 1 and Figure 5).

No specific explanation or guidance is provided of how "***the state machine 78 is built by a plurality of flip-flops***." As such, the claims contain "***state machine***" subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

7. The remaining claims 4, 5, 7, and 8 are rejected under 35 U.S.C. 112, second paragraph, as being dependent upon one or more rejected base claims.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. *Claims 1, 3-5, 7-10, and 19* are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***the display controller comprising...***" (lines 1-2); "***the converter comprising...***" (lines 4-5); "***the current mirror circuit comprising...***" (lines 9-10); and "***a voltage calibration circuit***" (line 17).

For example: It would be unclear to an artisan whether the "***voltage calibration circuit***" is intended to be a part of the earlier claimed "***current mirror circuit***," "***converter***," and/or "***display controller***."

11. Claim 1 is amenable to two or more plausible claim constructions.

The use of the phrase "***a current mirror circuit***" (line 6) renders the claim indefinite.

The claimed "***current mirror circuit***" is amenable to two plausible definitions.

Based on the description provided in the Specification, "***current mirror circuit***" could be interpreted to mean:

(a) The circuitry formed by the combination of transistors 82, 83a, 83b, and/or 83c in Figure 3 (*e.g., see Paragraph 17*).

(b) The circuitry formed by the combination of transistors 82, 83a, 83b, 83c, and/or voltage calibration circuit 68 in Figure 3 (*e.g., see Paragraphs 16-17*) -- wherein the voltage calibration circuit includes transistors 82, 88a, 88b, and 88c (*e.g., see Figure 4*).

Thus, neither the Specification, nor the claims, nor the ordinary meanings of the words provides any guidance as to what Applicant intends to cover with this claim language.

Due to the ambiguity as to what is intended by the claimed "***current mirror circuit***" and the fact that this claim element is amenable to two or more plausible claim constructions, this claim is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that the Applicant considers to be the invention.

See Ex parte Miyazaki (BPAI Precedential 19 November 2008).

12. The remaining claims are rejected under 35 U.S.C. 112, second paragraph, as being dependent upon rejected base claims.

13. The claims are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

As a courtesy to the Applicant, the examiner has attempted to also make rejections over prior art -- based on the examiner's best guess interpretations of the invention that the Applicant is intending to claim.

However, the indefinite nature of the claimed subject matter naturally hinders the Office's ability to search and examine the application.

Any instantly distinguishing features and subject matter that the Applicant considers to be absent from the cited prior art is more than likely a result of the indefinite nature of the claims.

The Applicant is respectfully requested to correct the indefinite nature of the claims, which should going forward result in a more precise search and examination.

Claim Rejections - 35 USC § 102 / 103

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. *Claims 1, 3-5, 7-10, and 19* are rejected under 35 U.S.C. 102(b) as anticipated by ***Dingwall (EP 780986 A2)***; or, in the alternative, under 35 U.S.C. 103(a) as obvious over ***Dingwall (EP 780986 A2)*** in view of ***Plus et al (US 5,170,155 A)***.

Regarding claim 1, ***Dingwall*** discloses a display controller [*e.g., Fig. 1*]

for driving a monitor [*e.g., Fig. 1: 16*], the display controller comprising:

a graphics chip [*e.g., Fig. 1: 11, 14, 21*]

for outputting [*e.g., Fig. 1: 22*] a display data [*e.g., Figs. 1, 2: W*]; and

a converter [*e.g., Figs. 1, 2: 23*]

for converting the display data into a display driving voltage [*e.g., Figs. 1, 2: OUT*],

the converter comprising:

a current mirror circuit [*e.g., Fig. 2: 110 (1-255), 111, 120(1-255)*]

for generating an output current [*e.g., Fig. 2: I123*]

according to a reference current [*e.g., Fig. 2: I111*] and the display data,

the output current and the reference current corresponding to a mirror ratio,

the output current being delivered to the monitor

for generating the display driving voltage,

the current mirror circuit comprising:

a first current route [*e.g., Fig. 2: 111*]

for delivering the reference current; and

a plurality of second current routes [*e.g., Fig. 2: 110 (1), 110 (2-3), 110 (4-7), 110 (8-15), 110 (16-31), 110 (32-63), 110 (64-127), 110 (128-255)*]

electrically connected to the first current route

for delivering a plurality of mirror currents [*e.g., Fig. 2: I110 (1), I110 (2-3), I110 (4-7), I110 (8-15), I110 (16-31), I110 (32-63), I110 (64-127), I110 (128-255)*]

to an output port of the converter [*e.g., Fig. 2: 124*]

to form the output current, wherein

the plurality of mirror currents have magnitudes differing from each other by a factor of two [*e.g., Fig. 2: I110 (2+3) = 2 x I110 (1),*

I110 (4+5+6+7) = 2 x I110 (2+3),

I110 (8+9+...+15) = 2 x I110 (4+5+6+7),

I110 (16+17+...+31) = 2 x I110 (8+9+...+15),

I110 (32+33+...+63) = 2 x I110 (16+17+...+31),

I110 (64+65+...+127) = 2 x I110 (32+33+...+63),

I110 (128+129+...+255) = 2 x I110 (64+65+...+127)], and

the plurality of mirror currents add together to form the output current; and

a voltage calibration circuit [*e.g., Fig. 2: 125, 130, 131, 143, 150*]

for modifying the mirror ratio

according to the display driving voltage and a reference driving voltage [*e.g., Fig. 2: VREF*] and

adjusting the output current

to drive the display driving voltage

to approach the reference driving voltage (*see the entire document, including Column 3, Line 13 - Column 7, Line 26*).

Should it be shown that ***Dingwall*** discloses the intended "*voltage calibration circuit*" with insufficient specificity; ***Plus*** is incorporated as a secondary/combinational reference.

Plus discloses additional details for making and using voltage calibration circuitry [*e.g., Figs. 1-3: 24*] for providing a display driving voltage approaching a desired display driving voltage (*see the entire document, including Column 2, Line 30 - Column 5, Line 65*).

Dingwall and ***Plus*** are analogous art, because they are from the shared inventive field of drive circuits for liquid crystal display devices. Moreover, ***Dingwall*** discloses the potential for combining together the inventions of the two references [*e.g., **Dingwall**: Column 1, Line 17; Column 4, Line 10*].

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Plus'*** comparator circuitry [*e.g., **Plus**: Figs. 1-3: 24*] with ***Dingwall's*** summation type digital-to-analog converter circuitry [*e.g., **Dingwall**: Figs. 1, 2: 23*]; so as to enhance the speed and accuracy of the combined display device [*e.g., **Plus**: Abstract*] while preventing any accuracy mismatch between the D/A converters [*e.g., **Dingwall**: Column 2, Line 31*]; resulting in the invention as instantly claimed.

Regarding claim 3, ***Dingwall*** discloses the voltage calibration circuit comprises:

a mirror ratio controller [*e.g., Fig. 2: 143-147*]

for controlling the mirror ratio;

a comparator [*e.g., Fig. 2: 131*]

for comparing the display driving voltage with the reference driving voltage

to generate a comparison result [*e.g., Fig. 2: ERROR*]; and

a state machine [*e.g., Fig. 2: 141, 142, 150, CP1, CP2*]

for generating a setting value [*e.g., Fig. 2: VCP1, VCP2*]

according to the comparison result and

outputting the setting value to the mirror ratio controller

to adjust the mirror ratio (*see the entire document, including Column 4, Line 14 - Column 7, Line 26*).

Regarding claim 4, ***Dingwall*** discloses the setting value is used for lowering the mirror ratio

if the display driving voltage is greater than the reference driving voltage, and

the setting value is used for raising the mirror ratio

if the display driving voltage is not greater than the reference driving voltage (*see the entire document, including Column 3, Line 13 - Column 7, Line 26*).

Regarding claim 5, ***Dingwall*** discloses the mirror ratio controller comprises

a plurality of mirror ratio setting units [*e.g., Fig. 2: 144-147*], and

the mirror ratio controller activates one or more of the plurality of mirror ratio setting units

according to the setting value

for adjusting the mirror ratio (*see the entire document, including Column 4, Line 14 - Column 7, Line 26*).

Regarding claim 7, ***Dingwall*** discloses the plurality of mirror ratio setting units correspond to a plurality of adjustment magnitudes

when adjusting the mirror ratio (*see the entire document, including Column 4, Line 14 - Column 7, Line 26*).

Regarding claim 8, ***Dingwall*** discloses each of the plurality of mirror ratio setting units is electrically connected to the first current route

through the current mirror circuit (*see the entire document, including Column 4, Line 14 - Column 7, Line 26*).

Regarding claim 9, ***Dingwall*** discloses the state machine enters a first operating state

for adjusting the setting value

to drive the mirror ratio controller

to lower the mirror ratio

if the comparison result corresponds to a first logic level, and

the state machine enters a second operating state

for adjusting the setting value

to drive the mirror ratio controller

to raise the mirror ratio

if the comparison result corresponds to a second logic level (*see the entire document, including Column 4, Line 14 - Column 7, Line 26*).

Regarding claim 10, ***Dingwall*** discloses the state machine will leave the first operating state and

enter a third operating state

for holding the setting value

if the state machine is presently at the first operating state, and

the comparison result corresponds to the second logic level, and

the state machine will leave the second operating state and

enter the third operating state

for holding the setting value

if the state machine is presently at the second operating state, and

the comparison result corresponds to the first logic level (*see the entire document, including Column 4, Line 14 - Column 7, Line 26*).

Regarding claim 19, ***Dingwall*** discloses the converter further comprises

a switch module [*e.g., Fig. 2: 113, 114, 120*] coupled to the plurality of second current routes

for controlling the plurality of second current routes respectively

to form the output current (*see the entire document, including Column 4, Line 14 - Column 7, Line 26*).

17. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Response to Arguments

18. Applicant's arguments filed 26 March 2009 have been fully considered but they are not persuasive.

The Applicant contends, "*Using flip-flops to built finite state machines is well known to those skilled in the art, and although paragraph [0032] does not describe the exact inter-connections needed in for the flip-flops, Figure 5 does clearly show the three states in the state machine 78. Therefore, the specification and figures enable one skilled in the art to make and use the invention including the state machine 78. As a result, the applicant believes that the subject matter of claims 3, 9, and 10 is described in the specification in such a way as to enable one skilled in the art to make and use the invention*" (see Page 7 of the Response filed 26 March 2009). However, the examiner respectfully disagrees.

No evidence has been provided supporting the Applicant's assertion that "*Using flip-flops to built finite state machines is well known to those skilled in the art.*"

The closest the originally presented specification ever comes to an enabling disclosure for making a "***state machine***" are the following two sentences: "***Generally speaking, the state machine 78 is built by a plurality of flip-flops. After the state machine 96 enters the operational state 96, the state machine, therefore, stops flip-flops from being triggered to achieve the objective of holding the setting value SET***" (see Paragraph 32, Line 1 and Figure 5).

No specific explanation or guidance is provided of how "***the state machine 78 is built by a plurality of flip-flops***." As such, the claims contain "***state machine***" subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The Applicant contends, "*The applicant believes that the line indentations, use of semi-colons, and use of the word 'and' clearly indicate which claimed elements are part of which structure. Therefore, the display controller comprises both a graphics chip and a converter. The converter comprises both a current mirror circuit and a voltage calibration circuit. The current mirror circuit comprises both a first current route and a plurality of second current routes. Therefore, the current mirror circuit means the circuitry formed by the combination of transistors 82, 83a, 83b, and 83c shown in Figure 3*" (see Page 8 of the Response filed 26 March 2009). However, the examiner respectfully disagrees.

An omitted structural cooperative relationship results from the claimed subject matter: "***the display controller comprising...***" (lines 1-2); "***the converter comprising...***" (lines 4-5); "***the current mirror circuit comprising...***" (lines 9-10); and "***a voltage calibration circuit***" (line 17).

For example: It would be unclear to an artisan (*reading only the pending claim language and not privy to the Applicant's above explanation*) whether the "***voltage calibration circuit***" is intended to be a part of the earlier claimed "***current mirror circuit***," "***converter***," and/or "***display controller***."

The claimed "***current mirror circuit***" is amenable to two plausible definitions. Based on the description provided in the Specification, "***current mirror circuit***" could be interpreted to mean:

(a) The circuitry formed by the combination of current mirror transistors *82, 83a, 83b, and/or 83c* in Figure 3.

(b) The circuitry formed by the combination of current mirror transistors 82, 88a, 88b, and/or 88c in Figure 4.

The Applicant contends, "***Dingwall*** *fails to disclose, teach or suggest 'the plurality of mirror currents having magnitude differing from each other by a factor of two' as recited in claim 1. Moreover,* ***Plus*** *fails to cure the deficiency neither*" (see Page 10 of the Response filed 26 March 2009). However, the examiner respectfully disagrees.

Dingwall discloses a current mirror circuit [*e.g., Fig. 2: 110 (1-255), 111, 120(1-255)*]

for generating an output current [*e.g., Fig. 2: I123*]

according to a reference current [*e.g., Fig. 2: I111*] and display data [*e.g., Figs. 1, 2: W*],

the output current and the reference current corresponding to a mirror ratio,

the output current being delivered to a monitor [*e.g., Fig. 1: 16*]

for generating display driving voltage [*e.g., Figs. 1, 2: OUT*],

the current mirror circuit comprising:

a first current route [*e.g., Fig. 2: 111*]

for delivering the reference current; and

a plurality of second current routes [*e.g., Fig. 2: 110 (1), 110 (2-3), 110 (4-7), 110 (8-15), 110 (16-31), 110 (32-63), 110 (64-127), 110 (128-255)*]

electrically connected to the first current route

for delivering a plurality of mirror currents [*e.g., Fig. 2: I110 (1), I110 (2-3), I110 (4-7), I110 (8-15), I110 (16-31), I110 (32-63), I110 (64-127), I110 (128-255)*]

to an output port of the converter [*e.g., Fig. 2: 124*]

to form the output current, wherein

the plurality of mirror currents have magnitudes differing from each other by a factor of two [*e.g., Fig. 2: I110 (2+3) = 2 x I110 (1),*

I110 (4+5+6+7) = 2 x I110 (2+3),

I110 (8+9+...+15) = 2 x I110 (4+5+6+7),

I110 (16+17+...+31) = 2 x I110 (8+9+...+15),

I110 (32+33+...+63) = 2 x I110 (16+17+...+31),

I110 (64+65+...+127) = 2 x I110 (32+33+...+63),

I110 (128+129+...+255) = 2 x I110 (64+65+...+127)], and

the plurality of mirror currents add together to form the output current

(*see the entire document, including Column 3, Line 13 - Column 7, Line 26*).

Dingwall discloses the current mirror circuitry being arranged in eight groups [*e.g., Fig. 2: 110 (1), 110 (2+3), 110 (4+5+6+7), 110 (8+9+...+15), 110 (16+17+...+31), 110 (32+33+...+63), 110 (64+65+...+127), 110 (128+129+...+255)*].

The current for each current mirror circuit group is summed together via respective switches [*e.g., 120*], so as to be double (i.e., "mirror currents have magnitudes differing from each other by a factor of two") the preceding current mirror circuit group's current.

For example: Group 2's summed current is double Group 1's current [*e.g., Fig. 2: I110 (2+3) = 2 x I110 (1)*], and

Group 3's summed current is double Group 2's current [*e.g., I110 (4+5+6+7) = 2 x I110 (2+3)*], etc.

Therefore, ***Dingwall*** does indeed disclose the plurality of mirror currents have magnitudes differing from each other by a factor of two, as instantly claimed.

Applicant's arguments with respect to *claims 1, 3-5, 7-10, and 19* have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
1 July 2009